Remarks

Reconsideration of this Application is respectfully requested.

Upon entry of the foregoing amendment, claims 1-5, 7-13, 17-25, 29-35, and 37-43 are pending in the application, with 1, 7, 13, 17-19, 24, 30, 32, 37, 39, 41, and 43 being the independent claims. Claims 1, 5, 7, 8, 11, 12, 13, 17-19, 24, 25, 29, 30, 32, 37, 39, and 41-43 are sought to be amended. These changes are believed to introduce no new matter, and their entry is respectfully requested.

Based on the above amendment and the following remarks, Applicants respectfully request that the Examiner reconsider all outstanding objections and rejections and that they be withdrawn.

Rejections Under 35 U.S.C. § 101

At page 2 of the Office Action, claims 1-5, 7-13, 17-25, 29-35, and 37-43 were rejected under 35 U.S.C. § 101:

> because the claimed invention is directed to non-statutory subject matter. With respect to claims 1, 7, 13, 17, 30, 32, and 41, the claims recite a transmission of a "signal" from a source to destination. According to MPEPE 2106.01 [R5] here in part;
>
> > "When nonfunctional descriptive material is recorded on some computer-readable medium, in a computer **or on an electromagnetic carrier signal**, it is not statutory since no requisite functionality is present to satisfy the practical application requirement.
>
> The "signal" presented in subject claims is simply an "electromagnetic signal" with no practical utility, and therefore making the claims non-statutory.
>
> Claims, 4-5, 8-13, 18-25, 29, 41, 33-35, 37-40, 42, and 43 are also rejected based on their dependency to a rejected base claim.

Applicants respectfully traverse these rejections.

Section 2106.01 of the Manual of Patent Examining Procedure recites, *inter alia*, "'[n]onfunctional descriptive material' includes but is not limited to music, literary works, and a compilation or mere arrangement of data." Hence, none of claims 1-5, 7-13, 17-25, 29-35, and 37-43 is directed to nonfunctional descriptive material.

Furthermore, Section 2106.01 of the Manual of Patent Examining Procedure also recites, *inter alia*:

> "functional descriptive material" consists of data structures and computer programs which impart functionality when employed as a computer component. (The definition of "data structure" is "a physical or logical relationship among data elements, designed to support specific data manipulation functions." The New IEEE Standard Dictionary of Electrical and Electronics Terms 308 (5th ed. 1993).)

Hence, none of claims 1-5, 7-13, 17-25, 29-35, and 37-43 is directed to functional descriptive material. Therefore, the Examiner's rejections under 35 U.S.C. § 101 have been misapplied. Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 1-5, 7-13, 17-25, 29-35, and 37-43 under 35 U.S.C. § 101.

Rejections Under 35 U.S.C. § 112

At page 3 of the Office Action, claims 10 and 11 were rejected under the first paragraph of 35 U.S.C. § 112:

> as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The subject claims recite here in part ". . . delay buffers to be configured one of to convey said first bit through said delay buffer and to bypass said first bit around said delay buffer". The language is vague and confusing, it is not clear from the specification or

drawings whether the "first bit" is being conveyed or bypassed. Appropriate correction is required.

Applicants respectfully traverse these rejections.

For example, in the present patent application, paragraphs [0133], [0134], and [0138] of the specification and amended figure 13A and figure 13B disclose how to use the features of the invention recited in claim 10 and amended claim 11. Paragraphs [0133] and [0134] recite:

> Pad delay circuit α.I.01 1102 comprises eight delay buffers: α.I.01.b1 1302, α.I.01.b2 1304, α.I.01.b3 1306, α.I.01.b4 1308, α.I.01.b5 1310, α.I.01.b6 1312, α.I.01.b7 1314, and α.I.01.b8 1316, seven multiplexers: α.I.01.m1 1318, α.I.01.m2 1320, α.I.01.m3 1322, α.I.01.m4 1324, α.I.01.m5 1326, α.I.01.m6 1328, and α.I.01.m7 1330, and three delay flip-flops: α.I.01.d1 1332, α.I.01.d2 1334, and α.I.01.d3 1336.
>
> The eight delay buffers are coupled in series: α.I.01.b1 1302 is coupled to α.I.01.b2 1304 at a node N_1 1338, α.I.01.b2 1304 is coupled to α.I.01.b3 1306 at a node N_2 1340, α.I.01.b3 1306 is coupled to α.I.01.b4 1308 at a node N_3 1342, α.I.01.b4 1308 is coupled to α.I.01.b5 1310 at a node N_4 1344, α I.01.b5 1310 is coupled to α.I.01.b6 1312 at a node N_5 1346, α.I.01.b6 1312 is coupled to α.I.01.b7 1314 at a node N_6 1348, and α.I.01.b7 1314 is coupled to α.I.01.b8 1316 at a node N_7 1350. The output of delay buffer α.I.01.b8 1316 is at a node N_8 1352.

Paragraph [0138] recites:

> Pad delay circuit α.I.01 1102 can receive a bit 1360 at an input 1362 and transmit bit 1360 at an output 1364. Each delay buffer delays bit 1360 as it traverses the interconnect. The multiplexers determine the number of delay buffers through which bit 1360 traverses en route to output 1364. FIG. 13B is a truth table 1380 that shows, as a function of the value of each of nodes N_9 1354, N_{10} 1356, and N_{11} 1358, the delay buffer node that is connected to output 1364. For example, truth table 1380 shows that if the value of each of nodes N_9 1354, N_{10} 1356, and N_{11} 1358 is, respectively, 1, 0, and 1, then node N_5 1346 is connected to output 1364. In this situation, bit 1360 received at input 1362 traverses through five delay buffers en route to output 1364. Thus, the degree to which bit 1360 is delayed can be adjusted in increments by changing the value of any of nodes N_9 1354, N_{10} 1356, and N_{11} 1358.

For example, in amended FIG. 13A, each of delay buffers α.I.01.b2 1304, α.I.01.b3 1306, α.I.01.b4 1308, α.I.01.b5 1310, α.I.01.b6 1312, α.I.01.b7 1314, and α.I.01.b8 1316 is

configured both to convey bit 1360 through the delay buffer and to bypass bit 1360 around the delay buffer as recited in claim 10.

Also, for example, in amended FIG. 13A, multiplexers α.I.01.m1 1318, α.I.01.m2 1320, α.I.01.m3 1322, α.I.01.m4 1324, α.I.01.m5 1326, α.I.01.m6 1328, and α.I.01.m7 1330, and delay flip-flops α.I.01.d1 1332, α.I.01.d2 1334, and α.I.01.d3 1336 comprise a control circuit configured to align delay buffers α.I.01.b2 1304, α.I.01.b3 1306, α.I.01.b4 1308, α.I.01.b5 1310, α.I.01.b6 1312, α.I.01.b7 1314, and α.I.01.b8 1316 to convey bit 1360 through a delay buffer or to bypass bit 1360 around a delay buffer as recited in claim 11.

Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 10 and 11 under the first paragraph of 35 U.S.C. § 112.

Rejections Under 35 U.S.C. § 102

At page 3 of the Office Action, claims 1-5, 13, 17, 24, 25, 29, and 32-35 were rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 4,627,070 to Champlin *et al.* (hereinafter "Champlin"). Applicants respectfully traverse these rejections.

Regarding claims 1-5, 13, 17, 24, 25, and 29, amended independent claim 1 recites (emphasis added):

> A cross link multiplexer bus, comprising:
>
> a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive ***a data signal*** and an origin port configured to produce said data signal; and
>
> a plurality of interconnects, wherein ***a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers*** of said plurality of cross link multiplexers;
>
> wherein a first interconnect of said set of interconnects has a first length, a second interconnect of said set of interconnects has a second length, and said first length and said second length are substantially equal;

> wherein ***said first interconnect is configured to convey a first bit of a number of bits of said data signal*** and ***said second interconnect is configured to convey a second bit of said number of bits of said data signal*** and said first bit remains substantially synchronized with said second bit.

Independent claims 13, 17, and 24 have been amended in a similar manner.

Champlin is directed to a bus system in which ***data are conveyed serially***, not in parallel. Champlin uses a single line, not a plurality of lines, to convey data. For example, Champlin, at column 7, lines 60-65, recites: "[t]he lines between the receiver portion of the T/R module **12** and the multiplex terminal and the lines between the transmitter portion of the T/R module and the multiplex terminal are each three in number, carrying a clock signal, a framing signal and data signals."

Therefore, Champlin does not anticipate any of amended independent claims 1, 13, 17, and 24. Because each of claims 2-5, 25, and 29 depends upon claims 1 or 24 and because of the additional distinctive features of each of claims 2-5, 25, and 29, each of these claims is also not anticipated by Champlin.

Regarding claims 32-35, amended independent claim 32 recites (emphasis added):

> A method for conveying a signal across a cross link multiplexer bus, comprising the steps of:
> (1) conveying the signal from a first cross link multiplexer of the cross link multiplexer bus to a second cross link multiplexer of the cross link multiplexer bus; and
> (2) at one of the first cross link multiplexer and the second cross link multiplexer, converting the signal from a first format to a second format;
> (3) synchronizing bits of a character of the signal;
> wherein the first format is one of a ***10 Gigabit Media Independent Interface protocol, a 10 Gigabit Attachment Unit Interface protocol, and a Converged Data Link protocol***, the second format is one of ***the 10 Gigabit Media Independent Interface protocol, the 10 Gigabit Attachment Unit Interface protocol, and the Converged Data Link protocol***, and the second format is different from the first format.

Champlin is not directed to a bus system that conveys data according to any of these protocols. Therefore, Champlin does not anticipate amended independent claim 32. Because

each of claims 33-35 depends upon claim 32 and because of the additional distinctive features of each of claims 33-35, each of these claims is also not anticipated by Champlin.

Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 1-5, 13, 17, 24, 25, 29, and 32-35 under 35 U.S.C. § 102(b).

Rejections Under 35 U.S.C. § 103

At page 5 of the Office Action claims 7-12, 30, 31, 41, and 42 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Champlin in view of U.S. Patent No. 6,137,734 to Schoner *et al.* (hereinafter "Schoner"). Applicants respectfully traverse these rejections.

Amended independent claim 7 recites (emphasis added):

> A cross link multiplexer bus, comprising:
> a plurality of cross link multiplexers, said plurality of cross link multiplexers having a destination port configured to receive ***a data signal***, at least one delay buffer configured to delay conveyance of said data signal, and an origin port configured to produce said data signal; and
> a plurality of interconnects, wherein ***a set of interconnects of said plurality of interconnects is coupled between a pair of adjacent cross link multiplexers*** of said plurality of cross link multiplexers;
> wherein ***a first interconnect of said set of interconnects is configured to convey a first bit of a number of bits of said data signal*** and ***a second interconnect of said set of interconnects is configured to convey a second bit of said number of bits of said data signal*** and said first bit remains substantially synchronized with said second bit.

Independent claims 30 and 41 have been amended in a similar manner.

Champlin, as stated above, is directed to a bus system in which ***data are conveyed serially***, not in parallel. Schoner is directed to a ***memory controller***, not a bus system.

A prima facie case of obviousness has not been established. Section 2143 of the Manual of Patent Examining Procedure recites, *inter alia*:

> To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary sill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

First, because Champlin is directed to a bus system in which data are conveyed serially, one of skill in the art would have no reason to refer to Schoner to incorporate a delay buffer into the bus system to synchronize the timing of data signals.

Second, rather than improve the performance of the bus system of Champlin, incorporation of a delay buffer into the data line of the Champlin bus system would degrade its performance by causing the data signals to lose synchronization with the clock signal and the framing signal. For example, as stated above, Champlin, at column 7, lines 60-65, recites: "[t]he lines between the receiver portion of the T/R module **12** and the multiplex terminal and the lines between the transmitter portion of the T/R module and the multiplex terminal are each three in number, carrying a clock signal, a framing signal and data signals."

Finally, neither Champlin nor Schoner, alone or in combination, discloses, teaches, or suggests a first interconnect, of a set of interconnects coupled between a pair of adjacent cross link multiplexers, configured to convey a first bit of a data signal and a second interconnect, of the set of interconnects coupled between the pair of adjacent cross link multiplexers, configured to convey a second bit of the data signal.

Therefore, each of amended independent claims 7, 30, and 41 is patentable over Champlin in view of Schoner. Because each of claims 8-12, 31, and 42 depends upon claims 7, 30, or 41 and because of the additional distinctive features of each of claims 8-12, 31, and 42, each of these claims is also patentable over Champlin in view of Schoner.

Accordingly, Applicants respectfully request that the Examiner reconsider and remove his rejections of claims 7-12, 30, 31, 41, and 42 under 35 U.S.C. § 103(a).

Allowable Subject Matter

At page 7 of the Office Action, claims 18-23, 37-40, and 43 "are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Accordingly, Applicants have amended each of claims 18 and 19 to incorporate the features of independent claim 17. Each of claims 20-23 remains dependent upon claim 19. Applicants have also amended each of claims 37 and 39 to incorporate the features of independent claim 32. Claim 38 remains dependent upon claim 37 and claim 40 remains dependent upon claim 39. Applicants have also amended claim 43 to incorporate the features of independent claim 41 and intervening claim 42.

Therefore, Applicants respectfully request that the Examiner reconsider and remove his objections to claims 18-23, 37-40, and 43 and pass these claims to allowance.

Amendments to Figure 13A

Applicants have amended Figure 13A, a schematic diagram of an embodiment of pad delay circuit α.I.01 1102, to add reference label "1362" for the input and reference label "1364" for the output. Support for these amendments can be found, *inter alia*, at paragraph [0138] of the specification.

Information Disclosure Statement

Applicants respectfully request that the Examiner indicate his consideration of the documents identified on the Forms PTO/SB/08A and PTO/SB/08B included with the Information Disclosure Statement filed on May 8, 2007.

Conclusion

All of the stated grounds of objection and rejection have been properly traversed or accommodated. Applicants therefore respectfully request that the Examiner reconsider all presently outstanding objections and rejections and that they be withdrawn. Applicants believe that a full and complete reply has been made to the outstanding Office Action and, as such, the present application is in condition for allowance. If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided.

Prompt and favorable consideration of this Amendment and Reply is respectfully requested.

Respectfully submitted,

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FIG. 13B
1380

Output								
N_9	N_{10}	N_{11}	N_1	N_2	N_3	N_4	N_5	N_6	N_7	N_8
0	0	0								
0	0	1								
0	1	0								
0	1	1								
1	0	0								
1	0	1								
1	1	0								
1	1	1								

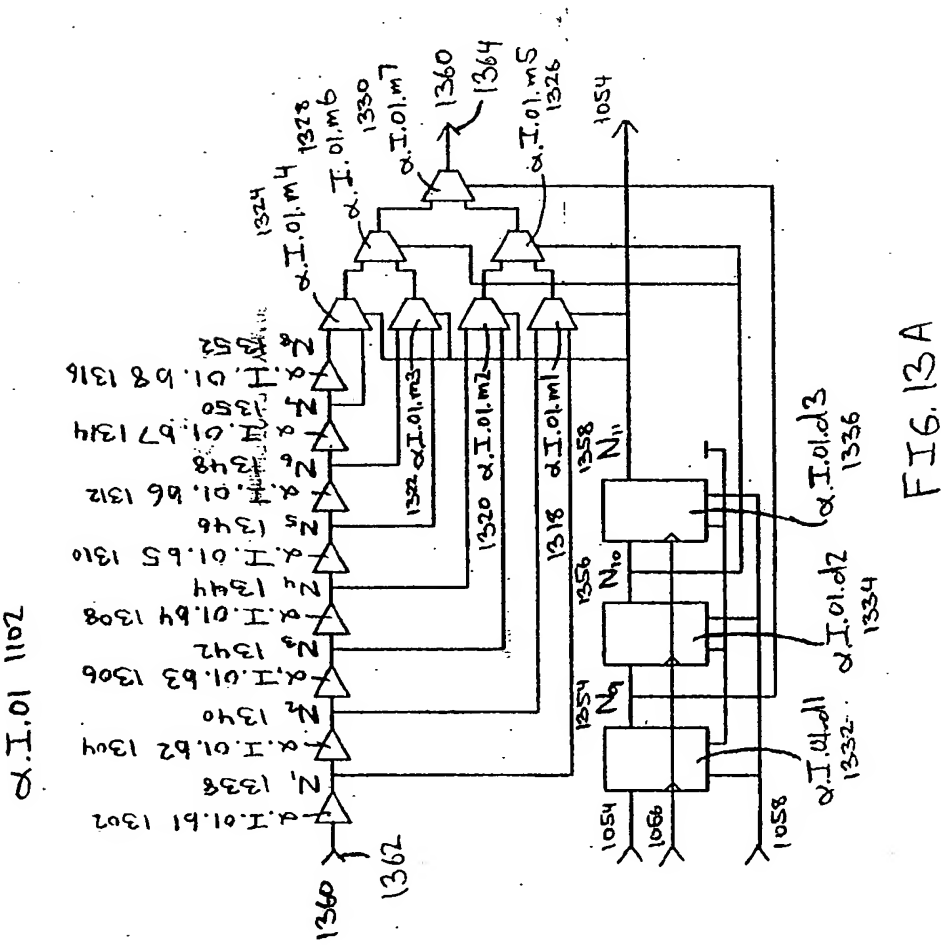

FIG. 13A